LESSON PLAN

Period	Date (Tentative)	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
	18/6/13	Introduction to logic families				
	19/6/13	CMOS logic				
	24/6/13	CMOS steady state electrical behaviour				
1	25/6/13	CMOS dynamic electrical behaviour				
2	1/7/13	CMOS logic families				
	6/7/13	Diode logic UNIT-II Bipolar logic				
	7/7/13	Transistor logic				
	9/7/13	TTL families				
	10/7/13	CMOS/TTL interfacing				
	10/7/13	low voltage CMOS logic and interfacing				
	13/7/13	emitter coupled logic				
	15/7/13	Comparision of logic families				
	17/7/13	Familarity with standard 74xx and CMOS 40xx IC specifications				
		UNIT-III				
	19/7/13	Introduction Design and Analysis procedures				
	22/7/13	Decoders using digital ICs				
	24/7/13	encoders using digital ICs				
	24/7/13	three state devices				
	26/7/13	multiplexers & demultiplexers				
		code converters				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
	16/8	Ex-OR gates and parity circuits				
	26/8	Comparators, adders & subtractors				
	26/8	Design & consideration of logic circuits using ICs				
		UNIT - IV				
	28/8/17	Ripple Adder, Carry generator				
	29/8/17	Binary parallel Adder				
	9/9/17	n-Bit parallel Subtractor				
	10/9/17	Binary adder Subtractor				
	11/9/17	ALU's, Combinational multipliers				
	16/9/17	Barrel Shifter Simple Floating point				
	18/9/17	Cascading comparators using Digital ICs				
	18/9/17	Dual priority Encoder with IC				
		UNIT - V				
	20/9/17	Introduction & Basic Bistable element Logic circuit using IC				
	20/9/17	Latches, Flip flops using Digital ICs				
	16/10/17	Flip-flop conversions				
	12/10/17	SSI latches & flip-flops.				
	12/10/17	Counters, & Design of counters using Digital ICs				
	24/10/17	Applications of counters Synchronous design methodology				
	24/10/17	Impediments to synchronous design				

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Period	Date (Tentative)	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
	26/12/17	Sequential Logic circuits with relevant ICs				
		UNIT - VI				
	29/12/17	MSI Registers Logic Circuits with Digital ICs				
	2/1/18	Using Relevant ICs Shift Register				
	3/1/18	modes of operation of Shift Registers				
	5/1/18	Universal shift Register using Digital ICs				
	5/1/18	MSI Shift Registers using Digital ICs				
	6/1/18	Ring counter explanation Operation.				
	6/1/18	Johnson Counter using IC				
	8/1/18	Basic Sequential Logic Design steps				
	8/1/18	Design of modulus N Synchronous counters using IC				
		UNIT - VII				
	9/1/18	Introduction to PLDs.				
	11/1/18	programmable Read only memory				
	12/1/18	programmable logic Array & PLDs with relevant ICs				
	12/1/18	Programmable Array Logic Devices				
	13/1/18	programmable Array Logic Devices using relevant IC				
	17/1/18	Comparision between PROM, PLA & PAL.				
	18/1/18	Comparision between PROM and PLA with relevant ICs				
	19/1/18	Comparision between PLA & PAL with relevant IC				

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Period	Date (Tentative)	Topic	Unit No	Teaching Methodology/	Remarks	[illegible] Upon Review
		UNIT VIII				
	16/11/17	Internal structure and 2D decoding of the ROM				
	17/11/17	Commercial types of the ROM				
	18/11/17	Timing and application of the different types of ROM				
	19/11/17	Internal structure of the static RAM				
	19/11/17	SRAM timing				
	20/11/17	Explanation of standard SRAMs				
	22/11/17	Synchronous SRAMs				
	23/11/17	Internal structure of the Dynamic RAM and timing specifications				
	23/11/17	Synchronous of DRAMs familiarity with data sheets, & specifications				[illegible]